

Code: EC5T3

III B.Tech - I Semester–Regular Examinations December 2016

**COMPUTER ARCHITECTURE AND ORGANISATION
(ELECTRONICS AND COMMUNICATION ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

- a) Describe the arithmetic shift micro operations of a computer .
- b) What is instruction register and program counter used for ?
- c) Compare Hardwired control and micro programmed control unit.
- d) What are condition code flags? What are the commonly used condition flags?
- e) Explain the term memory bus bottleneck.
- f) State the factors considered in designing an I/O subsystem.
- g) Give some examples where double precision calculations are needed.
- h) Indicate the types of hazards in instruction pipe lining.
- i) Signify how parallel processing improves the performance of a computer?
- j) What is locality of reference?

k) Draw the flowchart for adding and subtracting numbers in signed-2's complement representation.

PART – B

Answer any **THREE** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction. 8 M
- b) Justify the statement Hardwired control unit is faster than microprogrammed control unit. 8 M
3. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. 16 M
4. a) Differentiate RISC and CISC computers. 6 M
- b) Explain RISC pipelining. 10 M
5. Draw the flowchart of Booth's multiplication. Show the step by step process of Booth's multiplication algorithm for the numbers $(-14) * (+12)$. 16 M

6. Write short notes on
- a) Parallel Processing. 4 M
 - b) Pipe lining. 4 M
 - c) RISC Pipeline. 4 M
 - d) Vector Processing. 4 M